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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/999,663	12/18/97	COLGAN E	YO994-065XX

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EXAMINER	
DUDEK, J	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/999,663	Applicant(s) Colgan et al
	Examiner James Dudek	Group Art Unit 2871

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *three* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-14* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-14* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, on lines 7, the term "its electrodes" lacks the proper antecedent basis. Also, the term "a plurality of liquid crystal devices postitioned over respective mirrors on a dielectric layer on a semiconductor layer" is indefinite for many reasons such as it is unclear if the devices are on the dielectric layer or the mirrors are on the dielectric layer and the term "the liquid crystal devices" is a term that is not consistant with the termonology of the art.

In claim 4, on lines 3-5, the term "...a respective metal layer for reflecting light on said substantially planar upper surface of said supporting layer" is confusing because it is unclear how light can be on a substantially planar surface.

In claim 6, on lines 3-4, the term "a dielectric layer" is not distinct from the dielectric layer in claim 1. Furthermore, the claimed dielectric layer is under the mirror not over unless applicant is referring to the liquid crystal layer as the dielectric layer in which case the applicant needs to clearly write the claim to indicate that. Finally, the openings in a dielectric layer over the mirrors is confusing because applicant has not described any dielectric layer over the mirrors with openings.

In claim 14, on line 24, the term "said overlapping mirror" lacks the proper antecedent basis and on line 26 "said mirror" lacks the proper antecedent basis. Also, the term "the liquid crystal devices" is a term that is not consistant with the termonology of the art.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

5. Claims 1 and 3-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyawaki et al (5,708,486).

Miyawaki et al disclose a spatial light modulator array for modulating light to form an image comprising: a plurality of liquid crystal devices (the volume of liquid crystal that corresponds to the region above pixel electrodes) positioned over respective mirrors (11) on a dielectric layer (13) on a semiconductor substrate (1), a plurality of electrical circuits (3-8) formed in said semiconductor substrate (see figures) coupled to said liquid crystal devices, respectively, for placing a voltage across its electrodes (coupled via the electric field generated by the pixel electrodes), and a reflector/absorber layer (12) positioned and patterned with respect to said mirror for shielding said plurality of electrical from ambient light circuits (see figures, the shading layer clearly shields the transistor from the ambient light), said reflector/absorber layer having an edge overlapping an edge of said mirror to form an overlapping region to decrease ambient light from passing into said semiconductor substrate (see figures).

Per claim 3, the mirrors are formed from aluminum (see column 2, lines 47-48).

Per claim 4, the mirrors have a supporting layer (13 and 21 of figure 9) having a substantially planar upper surface and the mirrors include a metal layer for reflecting light (the aluminum pixel electrode). Regarding the following limitation "a respective metal layer for

reflecting light on said substantially planar surface of said supporting layer", since it unclear what the this limitation means, the examiner is unable to apply art. However, if applicant is referring to the reflection of light from the reflector/absorber to the under side the reflecting mirror then Miyawaki et al would inherently reflect light that way.

Per claim 5, the supporting layer includes a dielectric material (see column 5, lines 17-18 and column 10, line 51) and electrical vias (the hole in the insulator) for electrical connection to the metal layer.

Per claim 6, the plurality of liquid crystal devices have a thickness determined by a dielectric layer (13) having openings formed over said respective mirrors (the holes for connecting the mirrors). The thickness of the liquid crystal devices is determined by many factors including the pixel capacitance and the storage capacitance thus it is necessary to consider the thickness of the liquid crystal layer in accordance with the thickness of the dielectric layer.

Per claim 7, the dielectric layer is formed from a SiO_2 material, see column 5, lines 17-18.

Per claim 8, the respective mirrors form the lower electrode of the plurality of liquid crystal device and is electrically coupled to the output of the electrical circuits (see 11 of figure 9).

Per claim 9, the reflector/absorber is form from a Ti (see column 2, line 59).

Per claim 10, see figure 9; the reflector/absorber layer is electrically conductive (Ti) and forms a blanket over the semiconductor substrate with openings.

Per claim 11, see column 4, line 67; CMOS transistors are used.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 2, 12-13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyawaki et al.

Per claim 14, Miyawaki et al discloses a method of forming a spatial light modulator array comprising the steps of forming a plurality of electrical circuits in a semiconductor substrate positioned for interconnecting with subsequently formed liquid crystal devices, respectively (3-10 of figure 9), forming one or more layers of interconnections above the electrical circuits (11), forming a first dielectric layer over the electrical circuits (21), planarizing the first dielectric layer (see figure 9), forming a reflector/absorber layer of conductive material for shielding the electrical circuits (12), forming a second dielectric layer (13), forming studs through said second dielectric layer for electrical connection the subsequently formed mirrors (10 and 11), forming mirrors (11) over the dielectric layer (see figure 9), the mirrors overlapping the reflector/absorber layer to form a capacitor (see column 5, lines 11-19) and to attenuate light, applying a layer of liquid crystal material, orienting liquid crystal (inherent; the liquid crystal will necessarily be oriented to function) and forming a top electrode. Since the method of manufacturing the device is merely a list of forming each component and each component must be formed to make the device, the method of manufacturing would be inherent to the device. Miyawaki et al discloses the claimed invention, as described above, except for the spacers. However, it was notoriously well known to incorporate spacers in liquid crystal display in order maintain an even liquid crystal layer over the pixel regions. Therefore, it would have been obvious to one of ordinary skill in the art at the time

the invention was made to incorporate a spacer in the display of Miyawaki et al in order to maintain an even liquid crystal layer which would improve contrast.

Per claims 2, 12 and 13, Miyawaki et al disclose the claimed invention, as described above, except for the overlap of 5.4 microns, the capacitance of 0.03 pf and the pitch of 17 microns. However, it was well known to use a pixel pitch of 17 microns in order to improve the resolution. Also, when a pitch of 17 microns is incorporated into the display of Miyawaki et al the end result would produce of capacitance of 0.03 pf and an overlap of 5.4 microns because the same materials are used for Miyawaki et al that are the claimed materials and are the materials described in the specification, specifically the dielectric layer and both electrodes (for capacitance). The figures show the reflector/absorber overlapping almost the entire region under the mirror and thus would overlap by at least 5.4 microns. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a pixel pitch (which would necessary would produce a capacitance of 0.03 pf and an overlap of 5.4 microns) in the display of Miyawaki et al in order to improve the resolution.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Dudek at (703) 308-4093

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